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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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First Named Inventor or Application Identifier	
MCGLINCHEY, Gerard Francis	
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☑ Fee Transmittal Form
   (Submit an original, and a duplicate for fee processing)
2. ☑ Specification [Total pages 19]
   14 pages specification
   1 pages abstract
   4 pages claims
   21 claims
3. ☑ Drawing(s) *(35 USC 113)* [Total sheets 8]
   ☑ Informal Γ Formal [Total drawings 8]
4. ☑ Oath or Declaration [Total pages 2]
   a. ☑ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation by Reference
   (usable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & documents(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
   (when there is an assignee)
10. ☐ English Translation of Document *(if applicable)*
11. ☐ Information Disclosure Statement (IDS)/PTO-1449 Γ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☑ Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
    (if foreign priority is claimed)

16. Other:

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

☐ Cancel in this application original claims of the prior application before calculating the filing fee.

☐ Amend the specification by inserting before the first line the sentence:

This application is a ☐ continuation ☐ divisional of application serial no. , filed , entitled , and now .

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Attorney Docket No. T0461/7003 (SJH)

Inventor or Identifier: MCGLINCHEY, Gerard Francis

Serial No: Not yet assigned

Filed: Herewith

For: *FAST ETHERNET AND ETHERNET DRIVER*

CHECK BOX, if applicable:

☐ **DUPLICATE**

Fee Calculation Sheet

CLAIMS	FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
	TOTAL CLAIMS (37 CFR 1.16(c))	21-20=	1 x	$18	= $18.00
	INDEPENDENT CLAIMS (37 CFR 1.16(b))	4-3=	1 x	$78	= $78.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d)) +			$	= $0.00
				BASIC FEE (37 CFR 1 16(a))	$ 760.00
			Total of above Calculations =		$856.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				$856.00
	Assignment Recordation Fee (if any)				$ 0.00
	Other Fees (e.g., Petition for Extension of Time), if any **NOTE: Enter small-entity amount if applicable.**				$ 0.00
	TOTAL =				$856.00

1. A check in the amount of $856.00 is enclosed.

General Authorization to Charge Deposit Account and General Request for Extension of Time

2. a. ☑ If the filing of any paper in this application necessitates the payment of a fee under 37 CFR э ☑ 1.16 ☑ 1.17 or ☐ 1.18, and the fee due is in an amount different from any enclosed check or if no check is enclosed, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 23/2825.

   b. ☐ The applicant hereby revokes any prior authorization to charge a fee due under 37 CFR э ☐ 1.16 ☐ 1.17 or ☐ 1.18.

3. If the filing of any paper in this application necessitates an extension of time under 37 CFR э1.136(a), the applicant hereby requests such extension of time. If the fee due is in an amount different from any enclosed check or if no check is enclosed, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 23/2825.

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A FAST ETHERNET AND ETHERNET DRIVER

FIELD OF THE INVENTION

This invention relates generally to line driver circuitry and in particular to line drivers suitable for use in an Ethernet environment, and is more particularly directed toward a driver circuit for use with twisted pair cable in Ethernet and Fast Ethernet architectures.

BACKGROUND OF THE INVENTION

Ethernet™ is a network communication system developed and standardized by DEC, Intel, and Xerox using baseband transmission, Carrier Sense Multiple Access/Collision Detection (CSMA/CD) access, logical bus topology, and coaxial cable. A shared media network architecture, subsequently defined in the Institute of Electrical and Electronics Engineers (IEEE) 802.3 standard, it is currently the most popular architecture used in local area networks, and has been extended for operation using fiber optics, broadband, and unshielded twisted pairs. Ethernet is currently implemented using two main variants: Ethernet and Fast Ethernet.

The Ethernet or 10BaseT is a variant architecture based on the foregoing standard and operates up to 10Mbps

(megabits per second), using unshielded twisted pair cable (UTP). A 10BaseT architecture is also known as twisted pair Ethernet or UTP Ethernet. A second Ethernet standard, which includes implementations capable of 100Mbs transmission speeds, is defined in IEEE 802.3u, and is referred to as Fast Ethernet or 100Mbs Ethernet. A third implementation capable of 1Gbps (gigabit per second) transmission is currently being standardised.

The Ethernet™ system is used to link various nodes using a specific topology within a networked system, and initially utilised a coaxial cable with nodes tapped off the cable. A node is generally a device such as a personal computer, a workstation, server, bridge, or router, which is connected to the network at a single location. The topology is the logical pattern formed by the nodes of a network; i.e., the way the nodes are interconnected.

Topologies are either physical or logical. A physical topology is the configuration of nodes and links and describes the physical relationship between these nodes and links, whereas the logical topology describes which pairs of nodes are able to communicate and whether or not they have a physical connection. Local area networks (LANs) are usually configured in one of three topologies: star, ring, or bus.

Ethernet™ generally uses a star topology having nodes connected to a hub or switch box. The standard cable for use in both Ethernet and Fast Ethernet situations is a Category 5 (CAT5) cable, supporting transmissions up to 100Mbps, but also backwards compatible; i.e., can support 10Mbps transmissions. Each node may be connected to a hub using up to 100m of CAT5 cable.

In order to drive a signal over a network, it is necessary to use an Ethernet driver. In the star topology, the hubs or switches serve to restore a

signal's amplitude and timing between nodes, as it is not possible to drive a signal using Ethernet technology more than 100 meters before amplification is required.

Known Fast Ethernet (100BaseTx) and Ethernet (10BaseT) drivers can drive a signal up to 100 meters along CAT5 twisted pair cable. Drivers may be either current or voltage driven. Ethernet drivers typically require an output voltage with an accuracy of ±12%, whereas Fast Ethernet requires improved output voltage accuracy of ±5%.

Although it is possible to use a current source to drive both Ethernet and Fast Ethernet, it is preferable to use a voltage source to drive Fast Ethernet, as the accuracy levels achieved are much higher. It is possible for hubs to support exclusively Ethernet, exclusively Fast Ethernet, or both modes. All systems incorporate an Ethernet controller that determines the speed at which signals should be sent, and the standard describes how initial set-up is effected. For example, a hub may initially drive a card driver at Fast Ethernet speeds, and then check to see if a valid response is obtained. If it is not, then the hub will resend using Ethernet speeds.

Typically, the drivers are connected to the CAT5 cable by a 1:1 transformer and an RJ45 connector, and operate with a standard 3.3V power supply over a temperature range of 0^0C to 70^0C. An example of such an Ethernet driver is shown in FIG. 1.

The Ethernet driver 1 takes internal differential signals, inp and inn, and generates differential output signals capable of driving the CAT5 cable 2 in the manner previously described; i.e., by way of 1:1 transformer 3. The other end of the cable 2 connects to a second isolating 1:1 transformer 4, and the inputs 5 to an Ethernet receiver, rxp and rxn, are terminated in 50

Ohms. The source impedance at txp and txn is also 50 Ohms.

In the case of Fast Ethernet (100BaseTx), the MLT3 encoded differential output voltage (txp, txn) level is -1V to +1V. The Fast Ethernet data rate is 100MHz and the output voltage (txp, txn), accuracy is ±5%. The edge rates are limited to 4nS ±1nS to reduce radiation from the cable.

The Ethernet (10BaseT) output voltage (txp, txn) level is -2.5V to +2.5V. The Ethernet output voltage (txp, txn) accuracy is ±0.3V or ±12%. The signal is typically a Manchester encoded 10BaseT signal consisting of a 10MHz sine wave, which may be generated by a waveshaping circuit consisting of a look-up table and a digital-to-analog converter (DAC) followed by a low pass filter. The total harmonic distortion of the Ethernet signal is greater than 27dB.

Further examples of existing line driver architectures are shown in FIGS. 2, 3, and 4. FIG. 2 illustrates that a voltage source 11 may be used to drive the line. In this driver architecture, the source voltage (txp1, txn1) is two times the output voltage (txp, txn). In the case of a 3.3V power supply, this architecture can be used for Fast Ethernet where the source voltage is 2V, but not for Ethernet where the minimum output source voltage requirement is 4.4V. Other features shown include cable 12, transformers 13 and 14, and Ethernet receiver inputs 15.

As shown in FIG. 3, a current source 21 may be used to drive the line. The output currents develop the output voltage (txp, txn) directly across the line. In the case of a 3.3V power supply, this driver architecture can be used for both Fast Ethernet, where the output voltage is 1V, and also for Ethernet where the typical output voltage is 2.5V. Other features shown include

cable 22, transformers 23 and 24, and Ethernet receiver inputs 25.

A variation on the current driver is the use of a bridge current driver 31, as shown in FIG. 4. This driver includes four current sources, I1, I2, I3, and I4. The line termination resistors are now connected to an additional output voltage, Vmid. Vmid is half the supply voltage or 1.65V. This driver architecture uses 3 pins, but requires half the current of a two-pin current driver.

In the case of Fast Ethernet, each of the current sources, I1, I2, I3, and I4, is 20mA. A +1V (txp, txn) signal is generated when I4 sources 20ma, which flows through R1, R2 and L1 into I2. A 0V (txp,txn) signal is generated when the I4 current flows into I1 and the I3 current flows into I2. A -1V (txp, txn) signal is generated when I3 sources 20ma, which flows through R1, R2 and L1 into I1. In the case of Ethernet, the current levels are 50mA, generating a peak voltage (txp, txn) of 2.5V. Other features depicted in FIG. 4 include the cable 32, transformers 33 and 34, and receiver inputs 35.

In the early development of Ethernet, drivers were developed in single units. Although single drivers are still used in cards for installation at specific nodes, there is a requirement in hub design to increase the number of drivers that can be implemented on a single card. It is known in the prior art to provide quad drivers, wherein four drivers are implemented on a single card. Even though there has been a tendency toward hubs with 8, 16 or 32 ports, it has not been possible to improve upon the quad drivers already in existence. This is primarily due to the fact that the common power requirement of the drivers is such that if more than four drivers are implemented, the package power dissipation has been too high. There is, therefore, a need for

drivers with lower power dissipation, so as to facilitate the provision of multi-port drivers in hubs and switches.

SUMMARY OF THE INVENTION

These needs and others are met by the line driver circuit of the present invention, which has a reduced power requirement, and as such can be implemented in greater numbers on an integrated circuit than the well-known quad driver. The inventive line driver circuit is a combined Ethernet/Fast Ethernet driver circuit that incorporates the necessary current driver for Ethernet combined with the accuracy offered by a voltage driver for Fast Ethernet.

In accordance with one embodiment of the invention, a driver circuit for driving a line in a network comprises first driving means for driving the line, second driving means for driving the line, and switching means for switching between the first and second driving means. Preferably, the switching means operates to make only one of the first or second driving means active at any one time.

In one aspect of the invention, the switching means comprises a first input for enabling and disabling the first driving means and a second input for enabling and disabling the second driving means, wherein, when one of the first or second driving means is enabled, the other driving means is disabled. The first driving means may comprise one or more current sources, which may be connected in a bridge configuration.

In another form of the invention, the driver circuit is connected to a supply voltage and further comprises a plurality of terminating elements coupled to an output voltage of the driver circuit, wherein the driver circuit operates to limit the output voltage to about one-half of

the supply voltage. The second driving means may comprise a voltage source.

In yet another aspect of the present invention, a driver circuit for driving lines in a network comprises a plurality of current sources connected in a bridge configuration and coupled to the lines to provide a bridge current driver, a voltage source coupled to the lines to provide a voltage driver, and a plurality of terminating elements coupled to the current sources, the voltage source, and to the lines. The driver circuit further includes a supply voltage coupled to the bridge current driver and the voltage driver, wherein the supply voltage includes a mid-point termination voltage, and switching means for switching between the bridge current driver and the voltage driver, such that, when the bridge current driver is selected, the terminating elements are coupled to the mid-point termination voltage and the lines are driven from the bridge current driver. When the voltage driver is selected, the bridge current driver is disabled, and the terminating elements are coupled to the voltage driver. Preferably, the mid-point termination voltage is approximately equal to one-half the supply voltage, and the terminating elements comprise a network of resistors.

In still another aspect of the invention, a line driver circuit comprises a current source coupled to a first pair of terminals of a termination network and a voltage source coupled to a second pair of terminals of the termination network, wherein the voltage source operates in a first configuration to establish a first mode of operation, and in a second configuration to establish a second mode of operation. The current source may comprise a plurality of current sources. Preferably, the plurality of current sources are arranged in a bridge configuration.

The first mode of operation of the line driver circuit comprises voltage source drive mode. The first configuration of the line driver circuit corresponding to voltage source drive mode comprises driving the second pair of terminals of the termination network with the voltage source while the current source is maintained in an OFF state.

The second mode of operation of the line driver circuit comprises current source drive mode. The second configuration of the line driver circuit corresponding to current source drive mode comprises driving the first pair of terminals of the termination network with the current source while the voltage source maintains the second pair of terminals of the termination network at a predetermined, non-zero potential. The predetermined, non-zero potential preferably comprises one-half of line driver circuit supply voltage.

In still another form of the invention, the termination network comprises a resistive termination network. The resistive termination network preferably comprises a pair of resistors with the voltage source outputs coupled to a first end of each resistor and the current source outputs coupled to a second end of each resistor.

In accordance with yet another aspect of the invention, a method for providing multi-mode driver capability is described. The method comprises the steps of providing a line driver circuit including both a current source and a voltage source, selecting a first or second mode of operation, operating the line driver circuit in a first configuration when the first mode of operation is selected, and operating the line driver circuit in a second configuration when the second mode of operation is selected.

Further objects, features, and advantages of the present invention will become apparent from the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates an Ethernet driver circuit implementation that is known in the art;

FIG. 2 depicts a voltage driven line driver circuit of the prior art;

FIG. 3 shows a current driven line driver circuit of the prior art;

FIG. 4 shows a bridge current driven line driver circuit, in accordance with a known architecture;

FIG. 5 illustrates a Fast Ethernet and Ethernet driver in accordance with the present invention;

FIG. 6 is a schematic diagram of a cable driver in accordance with the present invention;

FIG. 7 is a schematic of a current feedback amplifier equivalent in accordance with the present invention; and

FIG. 8 is a schematic of a switched current feedback amplifier equivalent in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In accordance with the present invention, an Ethernet and Fast Ethernet driver is described that provides distinct advantages when compared to configurations known in the prior art. The invention may be implemented in a driver now described with reference to FIGS. 5 to 8, in which the Fast Ethernet driver has lower power than existing solutions, and the Ethernet bridge current generator is more accurate than

existing solutions. For existing architectures, the available power supply is 3.3V ± 5% or 3.165V to 3.465V. The operating temperature range is 0°C to 70°C.

FIG. 5 shows a Fast Ethernet and Ethernet driver according to the present invention. The driver allows both a voltage source drive 51 to be used for Fast Ethernet and a bridge current source drive 52 to be used for Ethernet. The driver architecture uses 4 pins, txp, txn, vp and vn. The expressions txp and txn are conventional terms for transmit positive and transmit negative respectively, while the expressions vp and vn indicate positive and negative termination voltages, respectively.

Line termination resistors 53, 54 connect to the two voltage sources, vp and vn. The two modes are combined by examining the termination resistors 53, 54, and having two inputs. By reconfiguring the termination resistors it is possible to implement either of the two modes. The choice of which mode is utilised is made using standard techniques such as those described previously.

In the case of Fast Ethernet, the bridge currents, (I1, I2, I3 and I4) are turned off, as will be described in greater detail subsequently with reference to FIG. 8, and the line is voltage driven from vp and vn. As Fast Ethernet is required, the txp, txn signal is 0.5V to -0.5V.

The line termination resistor r1 (53) is in series with r3 and r2 (54) is in series with r4. In order to obtain the required txp, txn signal, it is necessary to supply +1V, -1V at vp, vn. The load current is thus Vp/(r1+r3) or 1V/(100 Ohms); that is, 10mA. The presented voltage at vp, vn is such that a differential of 2V exists. As such, the on chip voltage drop is 3.3V - 2V or 1.3V. This results in an on-chip power dissipation of 1.3V*10mA, which is equal to 13mW.

In the case of Ethernet, the vp and vn voltages are set to an active mid-point termination voltage, vmid. Vmid is half the supply voltage or 1.65V for a 3.3V supply. The line is then driven from the bridge currents, I1, I2, I3, and I4. The line voltage is 2.5V with a resultant load current of 2.5V/50 Ohms, or 50mA. The on chip voltage drop is 3.3V - 2.5V or 0.8V, which equates to an on-chip power dissipation of 40mW.

This new architecture uses the accurate voltage drive to generate the Fast Ethernet's requisite ±5% accuracy signal, and the less accurate current drive to generate the Ethernet's ±12% accuracy signal. The Fast Ethernet signal is provided with a chip power dissipation of 13mW, which is lower than other known architectures. This results from lower on-chip voltages and load currents.

A current of 10mA is required to generate 0.5V across 50 Ohms. Known bridge current drivers, as described with reference to FIG. 4 above, use 20mA, as 10mA is delivered to the line and 10mA is required for across-the-line termination resistors. In the case of the single-ended current driver described with reference to FIG. 3, a 40mA current is required.

Comparisons of existing architectures with Ethernet and Fast Ethernet drivers in accordance with the present invention (termed "New Driver" in the Tables) are shown in Tables 1 and 2.

Table 1: Comparison of Fast Ethernet drivers

Architecture	Load Current	On Chip Voltage	Power Dissipation
Current Drive	40mA	2.8V	112mW
Bridge Current Drive	20mA	2.3V	46mW
New Driver	10mA	1.3V	13mW

Table 2: Comparison of Ethernet drivers

Architecture	Load Current	On Chip Voltage	Power Dissipation
Current Drive	100mA	0.8V	80mW
Bridge Current Drive	50mA	0.8V	40mW
New Driver	50mA	0.8V	40mW

A cable driver for the Fast Ethernet and Ethernet Driver of FIG. 5 is shown in the schematic of FIG. 6. The cable driver includes two current feedback amplifiers with a gain of -2. In Fast Ethernet mode, the logic input, Enable, turns off the Ethernet, or 10BaseT, output currents. The amplifier pamp2 controls the output voltages, vp and vn, and V(vp, vn) = V(txp,txn)*2.

The drivers in accordance with the present invention utilise a new method to generate the bridge currents. In FIG. 6, the 10BaseT current supplied to the line is from the outputs, Ioutp and Ioutn, of the amplifier pamp4, (see FIG. 8 for details). The currents Ioutp and Ioutn are ratios of the amplifier currents flowing in r3 and r4. In the case of pamp4, mp2 is 10 times the size of mp20, so the current in mp20 is 10 times the current in mp2. Ethernet driver circuits are conventionally biased from a fixed bandgap voltage, Vref, and an external resistor, Rext.

Ibias=Vref/Rext, a fixed current,

Vinp=Rinp*Ibias

Ir1=Vinp/r1=Rinp*Ibias/r1, a fixed current, since the ratio Rinp/r1 is constant

This current, Ir1, flows in r3 to outp of pamp4, and to either mp20 or mn20 in pamp4. A multiple of Ir1 flows to the line from mp2 or mn2 in pamp4 to Ioutp (FIG. 8). The voltage that is presented to the line at Txp is

Txp=r3*Ir1

If the absolute value of r3 is controlled to within ±12%, then the voltage on the line will be within the 10BaseT specification, and Txp will be a fixed voltage.

The input voltages inp, inn, inp1 and iin1 are derived from an on-chip reference voltage and an external resistor. For Fast Ethernet, the input voltage, (inp and inn) to the cable driver circuit is ±0.25V into 250 Ohms (1mA), and for Ethernet the input voltage drive is ±0.625V into 250 Ohms (2.5mA). The single-ended voltage gain of the amplifier, Txp/inp1, is r3/r1.

FIG. 7 is an equivalent circuit of the differential current feedback amplifier, pamp2, of FIG. 6. The amplifier signals are referenced to half the power supply voltage, Vmid = 1.65V. With two inputs and two outputs, the amplifier responds to the current input at inp and inn.

The pmos devices mp8, mp7, and mp6 connected to the voltage bias line vbiasp can be replaced by 3 current sources flowing from Vcc. Also, the nmos devices mn9, mn10, and mn11 connected to the voltage bias line vbiasn can be replaced by 3 current sources flowing to gnd. The input, vmid, is connected to a voltage source set between vcc and gnd or at 1.65V.

When the input, inp, is at the same voltage as the input, vmid, then no current flows in the input inp. When inp is below vmid, then there is a signal current flowing in mn1 in addition to the Imn9 current. This signal current is converted to a voltage gain at the gate of mp2. The current in mp2 increases providing a current at outp flowing from vcc to outp.

Also, when inp is below vmid, then the current flowing in mp1 is the Imn9 current minus the signal current. This signal current is converted into a voltage gain at the gate of mn2. The current in mn2 decreases, providing less current flowing from outp to gnd.

The amplifier will try to force the voltage at inp to match the voltage at inn by forcing more or less signal current into the inp input. Similarly, because it's a differential amplifier, it will also force inn to match vmid.

The switched current feedback amplifier pamp4 of FIG. 6 (illustrated in FIG. 8) is similar to the FIG. 7 amplifier except for the addition of a logic control, Enable, and the current outputs Ioutn and Ioutp. The logic input, Enable, switches the output of the amplifier.

When Enable is at gnd, enb is high and en is low. When en is low, the pmos switches mp9 and mp10 are on, which turns off the output currents flowing from Vcc to outp, Ioutp, outn and Ioutn. When enb is high, the nmos switches mn12 and mn13 are on, which turns off the output currents flowing from outp, Ioutp, outn and Ioutn to gnd. The auxiliary current outputs, Ioutp and Ioutn, match the current flowing in outp and outn.

When Enable is low, mp9, mp10, mn12, and mn13 turn on. This shuts off the output currents in mp2, mp20, mp4, mp40, mn2, mn20, mn4, and mn40. The currents in mp20, mp40, mn20 and mn40 are controlled by the current feedback amplifier pamp4. The Ethernet bridge currents, at mp2, mp4, mn2, and mn4, are a scaled version of the amplifier currents. In this particular implementation, the scaling factor is 10 times.

There has been described herein an Ethernet and Fast Ethernet driver which is improved over the prior art. It will be apparent to those skilled in the art that modifications may be made without departing from the spirit and scope of the invention. Accordingly, it is not intended that the invention be limited except as may be necessary in view of the appended claims.

What is claimed is:

CLAIMS

1. A driver circuit for driving a line in a network comprising:

first driving means for driving the line;

second driving means for driving the line; and

switching means for switching between the first and second driving means.

2. The driver circuit of claim 1, wherein the switching means operates to make only one of said first or second driving means active at any one time.

3. The driver circuit of claim 1, wherein the switching means comprises:

a first input for enabling and disabling the first driving means; and

a second input for enabling and disabling the second driving means;

wherein, when one of the first or second driving means is enabled, the other driving means is disabled.

4. The driver circuit of claim 1, wherein the first driving means comprises one or more current sources.

5. The driver circuit of claim 4, wherein said current sources are connected in a bridge configuration.

6. The driver circuit of claim 1, wherein the driver circuit is connected to a supply voltage and further comprises:

a plurality of terminating elements coupled to an output voltage of the driver circuit;

wherein the driver circuit operates to limit the output voltage to about one-half of the supply voltage.

7. The driver circuit of claim 1, wherein the second driving means comprises a voltage source.

8. A driver circuit for driving lines in a network comprising:

a plurality of current sources connected in a bridge configuration and coupled to said lines to provide a bridge current driver;

a voltage source coupled to said lines to provide a voltage driver;

a plurality of terminating elements coupled to the current sources, the voltage source, and to said lines;

a supply voltage coupled to the bridge current driver and the voltage driver, wherein the supply voltage includes a mid-point termination voltage;

switching means for switching between the bridge current driver and the voltage driver, such that, when the bridge current driver is selected, the terminating elements are coupled to the mid-point termination voltage and the lines are driven from the bridge current driver; and

when the voltage driver is selected, the bridge current driver is disabled and the terminating elements are coupled to the voltage driver.

9. The driver circuit of claim 8, wherein the mid-point termination voltage is approximately equal to one-half the supply voltage.

10. The driver circuit of claim 8, wherein the terminating elements comprise a network of resistors.

11. A line driver circuit comprising:

a current source coupled to a first pair of terminals of a termination network; and

a voltage source coupled to a second pair of terminals of the termination network;

wherein the line driver circuit operates in a first configuration to establish a first mode of operation, and in a second configuration to establish a second mode of operation.

12. The line driver circuit in accordance with claim 11, wherein the current source comprises a plurality of current sources.

13. The line driver circuit in accordance with claim 12, wherein the plurality of current sources are arranged in a bridge configuration.

14. The line driver circuit in accordance with claim 11, wherein the first mode of operation comprises voltage source drive mode.

15. The line driver circuit in accordance with claim 14, wherein the first configuration of the line driver circuit corresponding to voltage source drive mode comprises driving the second pair of terminals of the termination network with the voltage source while the current source is maintained in an OFF state.

16. The line driver circuit in accordance with claim 11, wherein the second mode of operation comprises current source drive mode.

17. The line driver circuit in accordance with claim 16, wherein the second configuration of the line driver circuit corresponding to current source drive mode comprises driving the first pair of terminals of the

termination network with the current source while the voltage source maintains the second pair of terminals of the termination network at a predetermined, non-zero potential.

18. The line driver circuit in accordance with claim 17, wherein the predetermined, non-zero potential comprises one-half of line driver circuit supply voltage.

19. The line driver circuit in accordance with claim 11, wherein the termination network comprises a resistive termination network.

20. The line driver circuit in accordance with claim 19, wherein the resistive termination network comprises a pair of resistors with the voltage source outputs coupled to a first end of each resistor and the current source outputs coupled to a second end of each resistor.

21. A method for providing multi-mode driver capability, the method comprising the steps of:

(a) providing a line driver circuit including both a current source and a voltage source;

(b) selecting a first or second mode of operation;

(c) operating the line driver circuit in a first configuration when the first mode of operation is selected; and

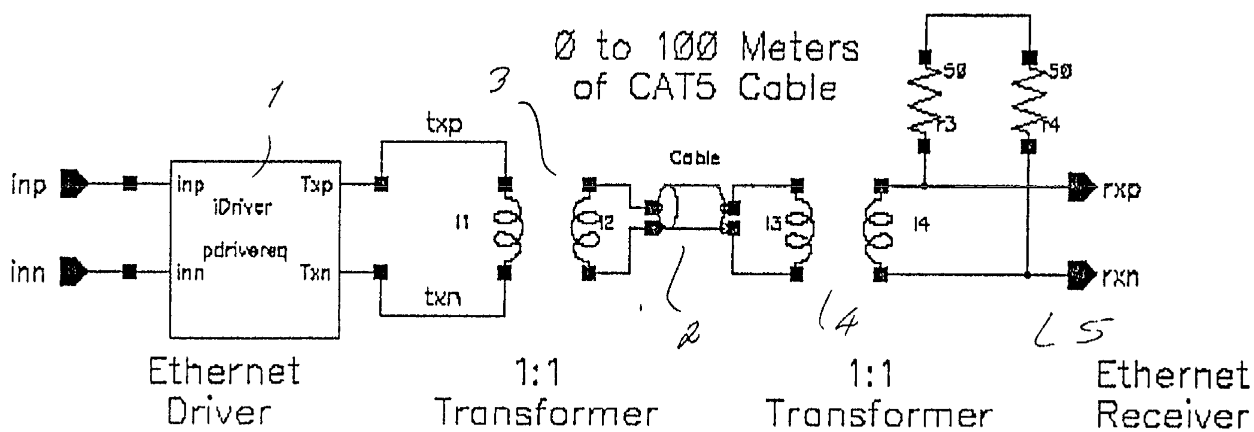
(d) operating the line driver circuit in a second configuration when the second mode of operation is selected.

A FAST ETHERNET AND ETHERNET DRIVER

ABSTRACT OF THE DISCLOSURE

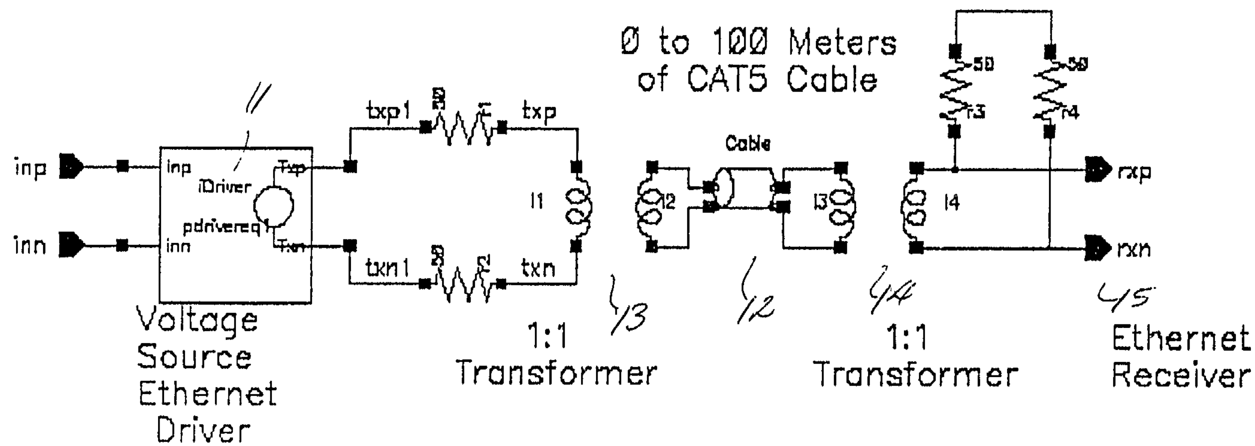
A driver circuit for driving a line in a network comprises first driving means for driving the line, second driving means for driving the line, and switching means for switching between the first and second driving means. A method for providing multi-mode driver capability is also described. The method comprises the steps of providing a line driver circuit including both a current source and a voltage source, selecting a first or second mode of operation, operating the line driver circuit in a first configuration when the first mode of operation is selected, and operating the line driver circuit in a second configuration when the second mode of operation is selected.

JH0073



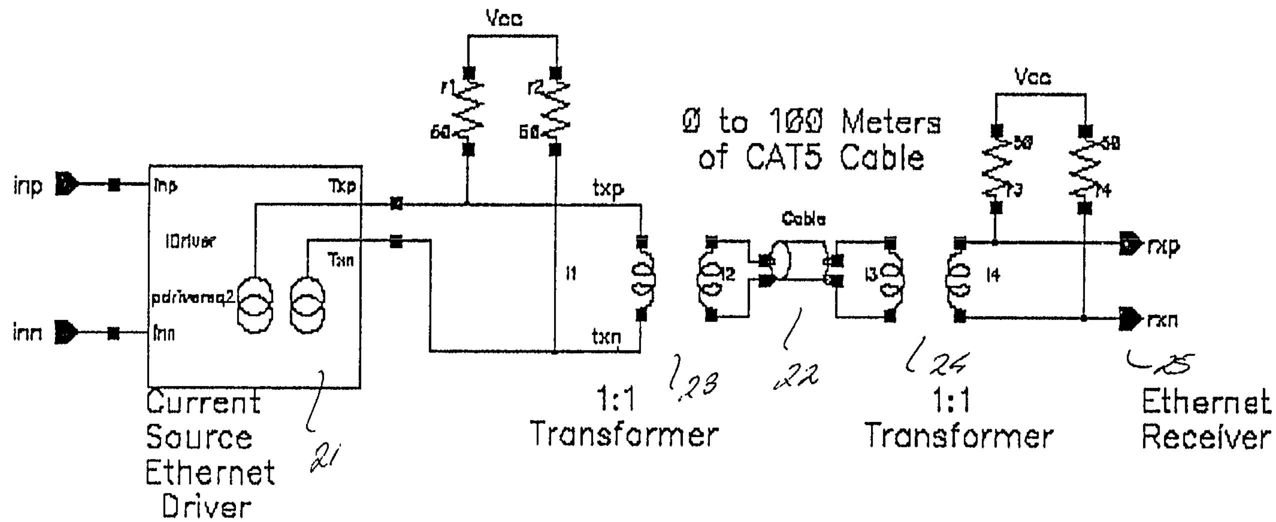
— PRIOR ART —

Fig 1



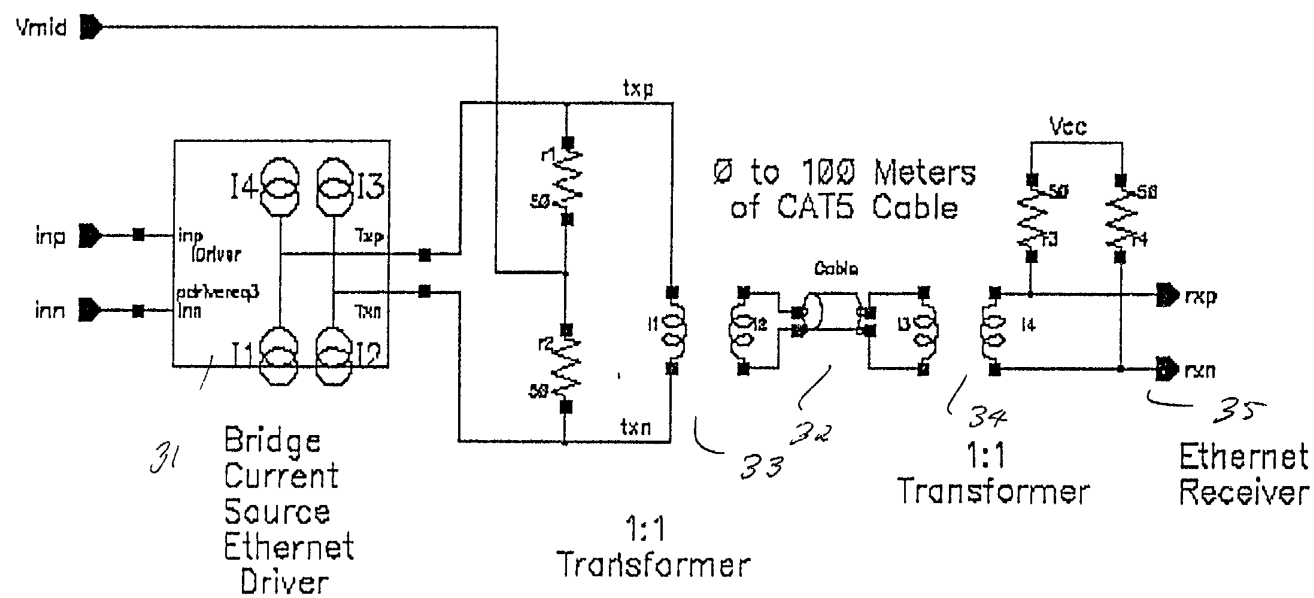
— PRIOR ART —

Fig 2



— PRIOR ART —

Fig. 3



— PRIOR ART —

Fig. 4

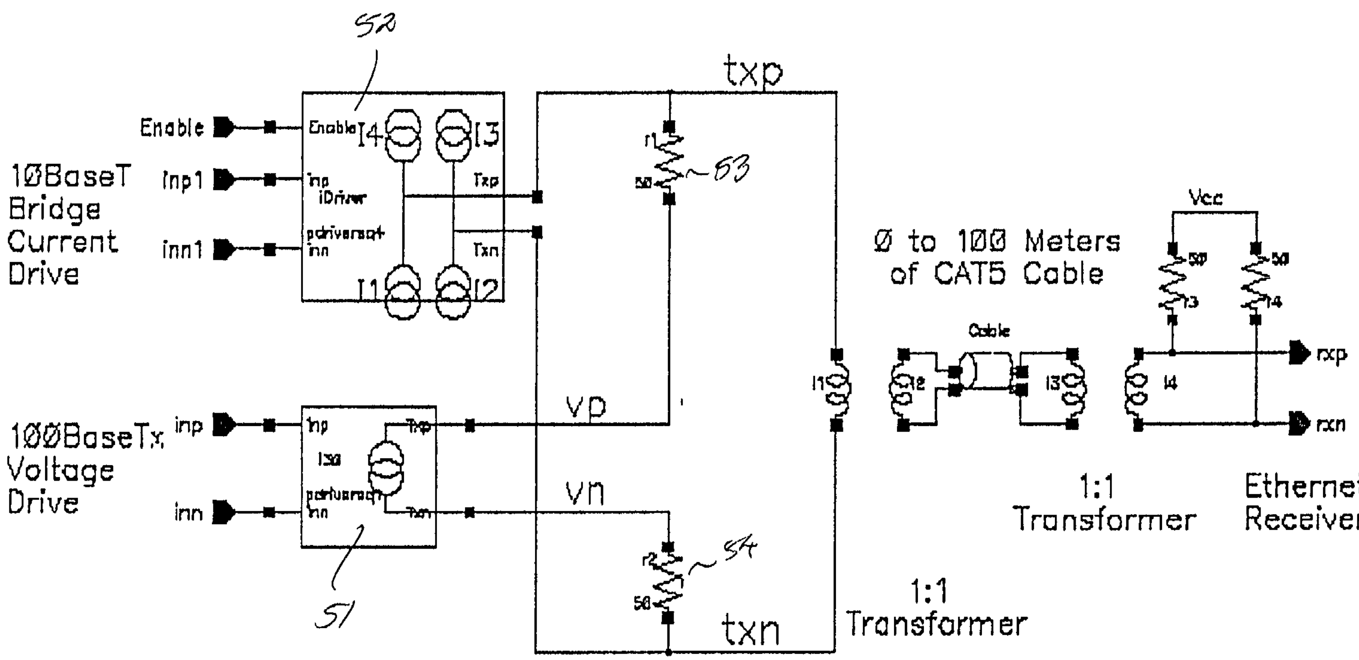
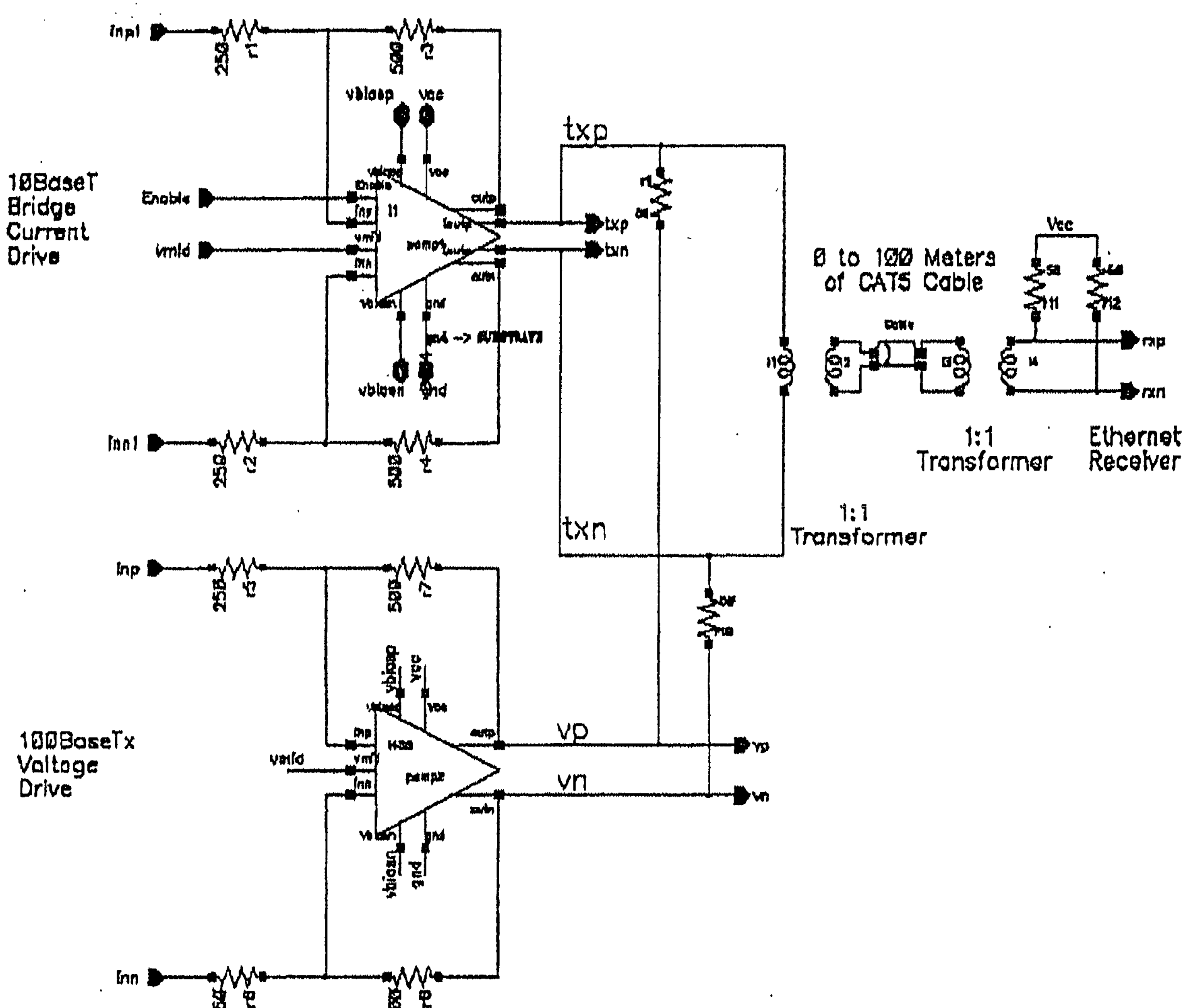

10BaseT
Bridge
Current
Drive
Enable
Inp1
inn1
100BaseTx
Voltage
Drive
inp
inn
52
51
53
54
txp
txn
vp
vn
Vcc
Cable
0 to 100 Meters
of CAT5 Cable
1:1
Transformer
1:1
Transformer
Ethernet
Receiver
rxp
rxn

Fig5



10BaseT Bridge Current Drive
100BaseTx Voltage Drive
0 to 100 Meters of CAT5 Cable
1:1 Transformer
1:1 Transformer
Ethernet Receiver
txp
txn
vp
vn
Inpl
Inn1
Inp
Inn
Enable
vmid
vbiasp
vcc
vbiasn
gnd
Vcc
rxp
rxn
250
500

Fig 6

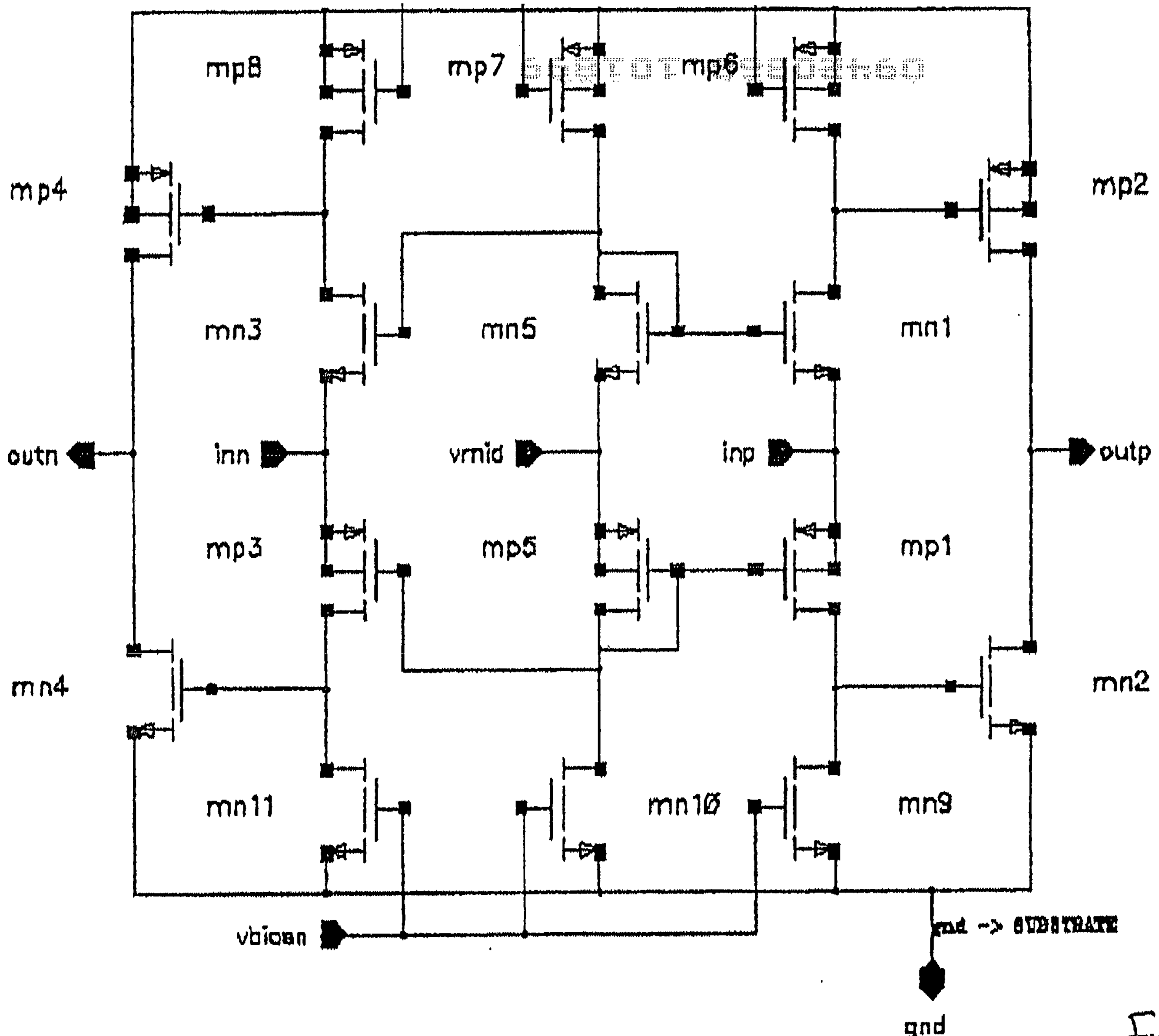

mp8
mp7
mp6
mp4
mp2
mn3
mn5
mn1
outn
inn
vmid
inp
outp
mp3
mp5
mp1
mn4
mn2
mn11
mn10
mn9
vbiasn
gnd -> SUBSTRATE
gnd

Fig 7

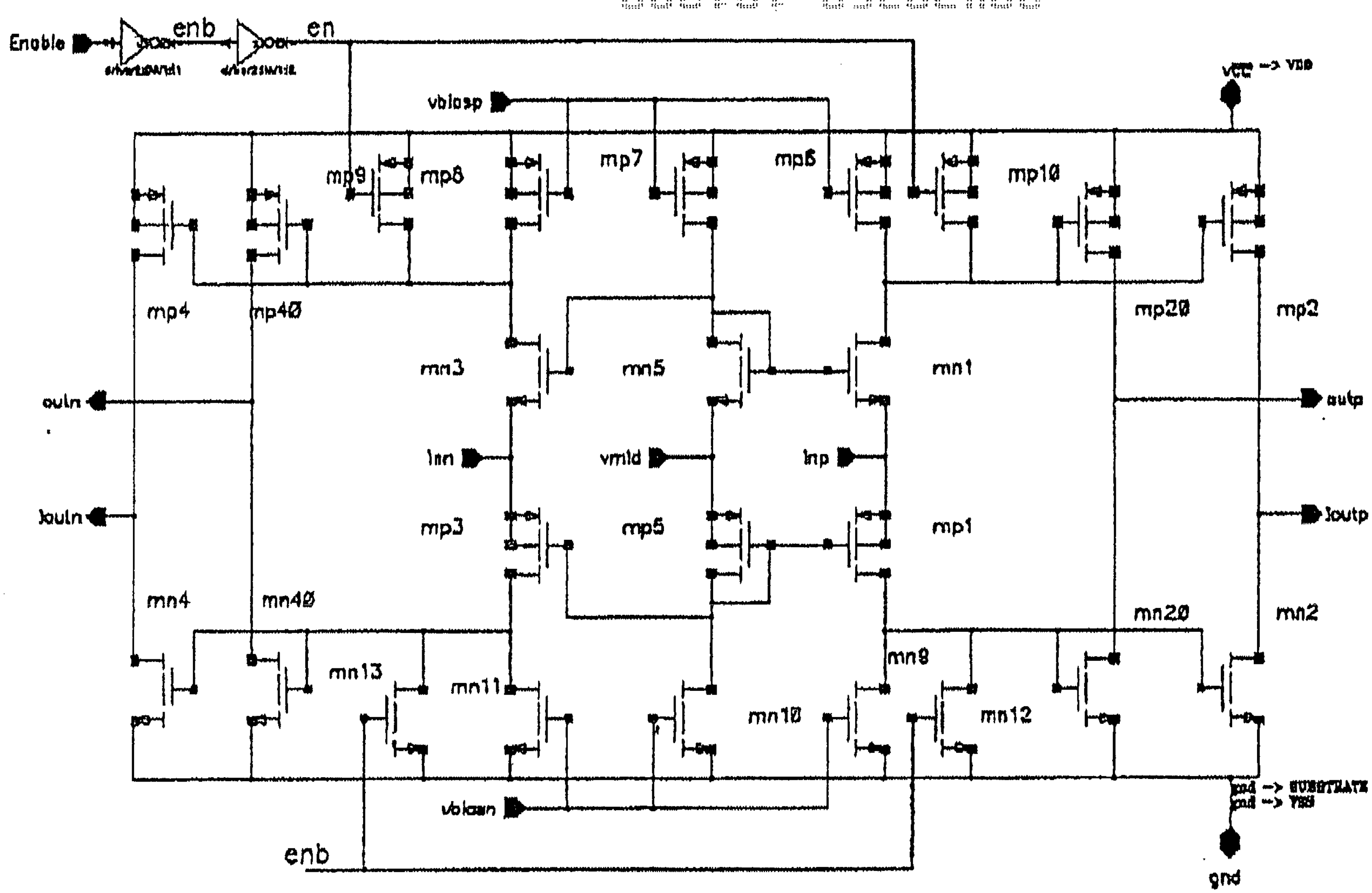

Enable
enb
en
vbiasp
vcc -> vdd
mp9
mp8
mp7
mp6
mp10
mp4
mp40
mp20
mp2
mn3
mn5
mn1
outn
inn
vmid
inp
outp
ioutn
ioutp
mp3
mp5
mp1
mn4
mn40
mn20
mn2
mn13
mn11
mn9
mn10
mn12
vbiasn
enb
gnd
gnd -> SUBSTRATE
gnd -> VSS

Figure 8

EXPRESS MAIL LABEL NO.: EM528920532US
Date of Mailing: October 18, 1999

Attorney Docket No. T0461/7003

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

FAST ETHERNET AND ETHERNET DRIVER

the specification of which is attached hereto unless the following is checked:

[ ] was filed on ______________, as United States Application No. ________________ (Include Series Code) or PCT International Application No. ______________________, bearing attorney docket No. ____________________, and was amended on ____________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or section 365(a) of any PCT International application designating at least one country other than the United States listed below and have also identified below any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign PCT International Application(s)and any priority claims under 35 U.S.C. §§119 and 365(a),(b):

			Priority Claimed	
(Number)	(Country-if PCT,so indicate)	(DD/MM/YY Filed)	[ ] YES	[ ] NO
(Number)	(Country)	(DD/MM/YY Filed)	[ ] YES	[ ] NO
(Number)	(Country)	(DD/MM/YY Filed)	[ ] YES	[ ] NO

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

(Application Number) (filing date)

(Application Number) (filing date)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or §365(c) of any PCT International application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application No.) (filing date) (status-patented, pending, abandoned)

PCT International Applications designating the United States:

(PCT Appl. No.)	(U.S. Ser. No.)	(PCT filing date)	(status-patented,pending,abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

G. M. Glinchey

Inventor's signature

15 OCT 1999

Date

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